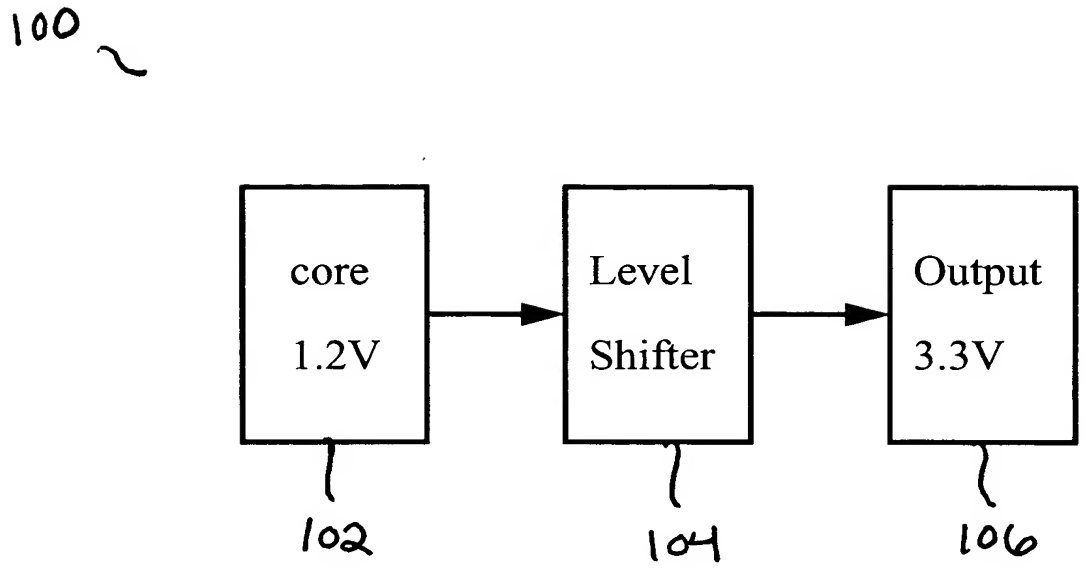

FIG. 1

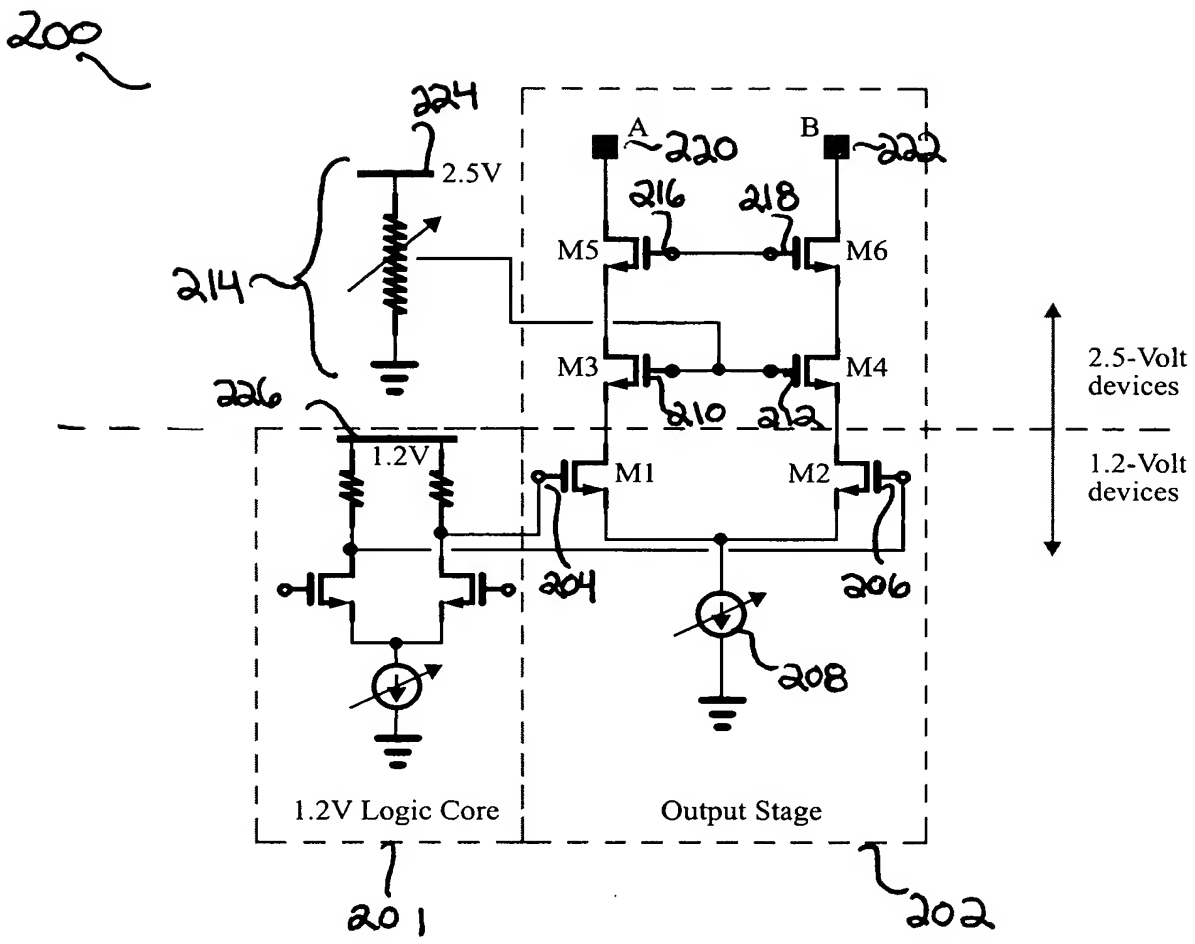
200
224
2.5V
214
226
1.2V
A
220
B
222
216
218
M5
M6
M3
M4
210
212
M1
M2
204
206
208
2.5-Volt devices
1.2-Volt devices
1.2V Logic Core
Output Stage
201
202

FIG. 2

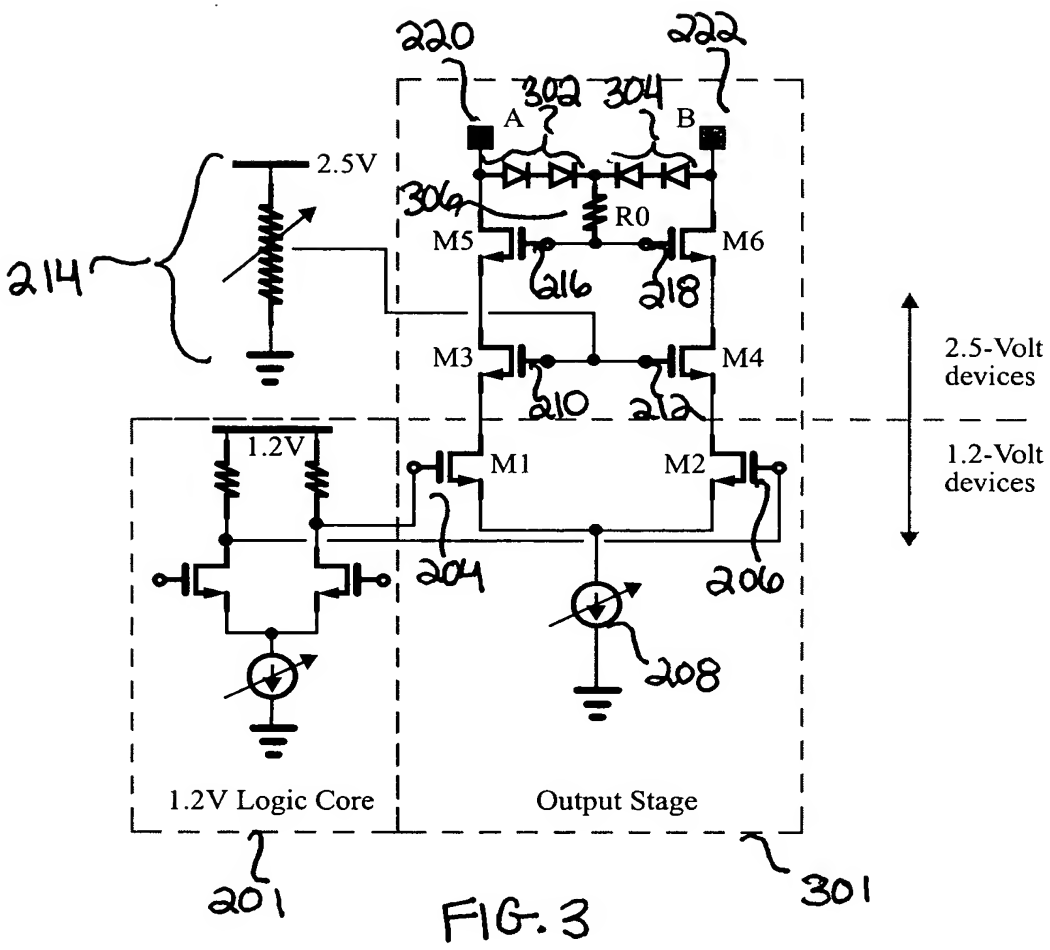
300
220
222
302
304
A
B
2.5V
306
R0
214
M5
M6
216
218
M3
M4
210
212
2.5-Volt devices
1.2V
M1
M2
1.2-Volt devices
204
206
208
1.2V Logic Core
Output Stage
201
301

FIG. 3

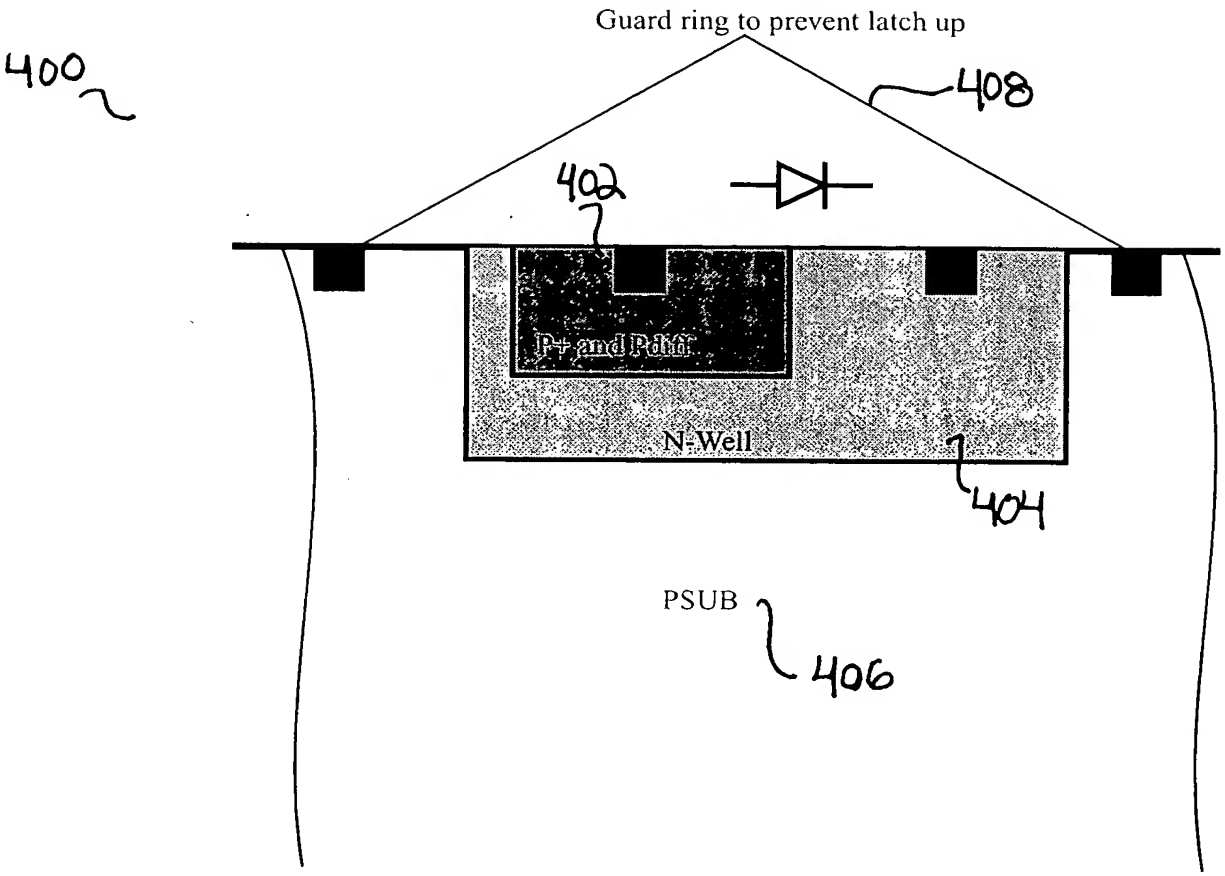
400
Guard ring to prevent latch up
408
402
P+ and Pdiff
N-Well
404
PSUB
406

FIG.4

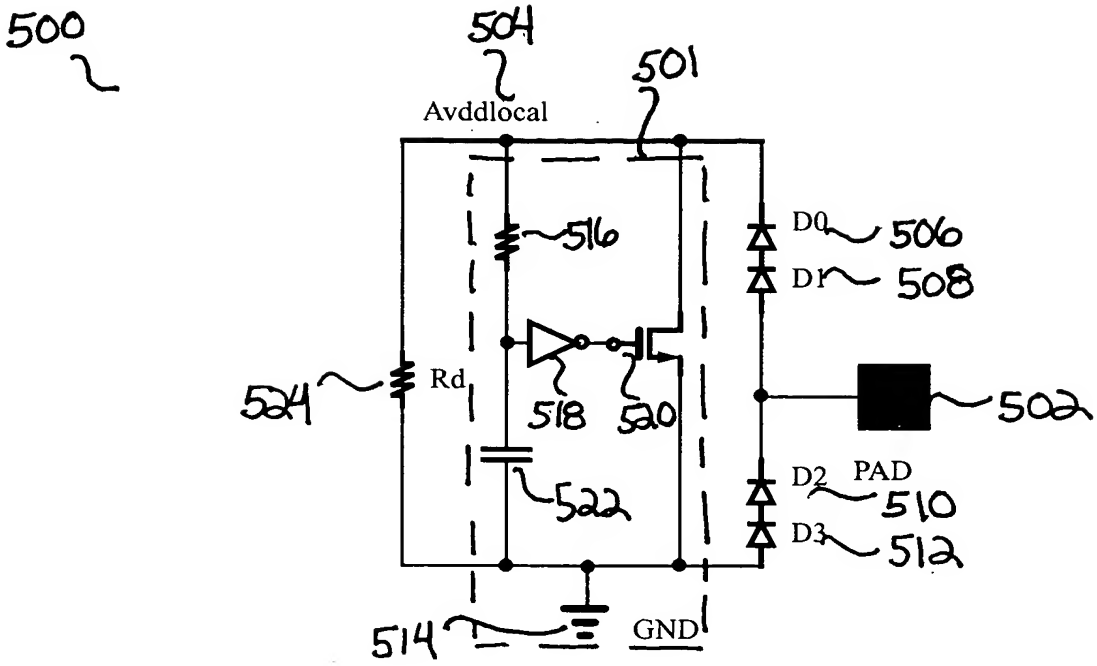
500
504
Avddlocal
501
516
D0
506
D1
508
524
Rd
518
520
502
522
D2
PAD
510
D3
512
514
GND

FIG. 5

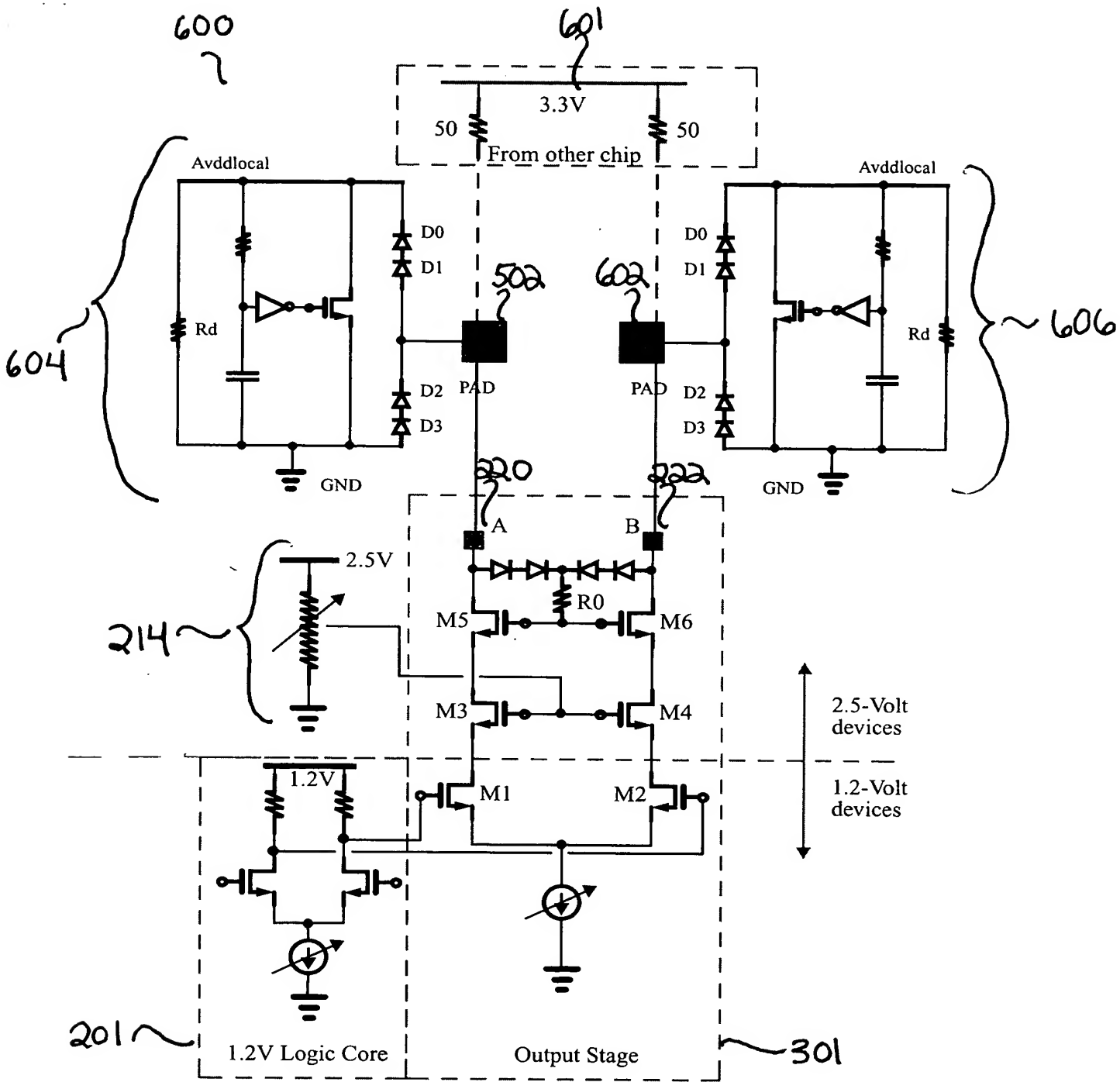
600
601
3.3V
50
50
From other chip
Avddlocal
Avddlocal
D0
D1
D2
D3
Rd
PAD
PAD
502
602
604
606
GND
GND
220
222
A
B
2.5V
214
R0
M5
M6
M3
M4
M1
M2
1.2V
2.5-Volt devices
1.2-Volt devices
201
1.2V Logic Core
Output Stage
301

FIG. 6